AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for moving an inverting buffer comprising:

interrogating a netlist, wherein the netlist comprises a source, a sink, and an inverting buffer associated with the source; and

moving thean inverting buffer from the sourcea source to the sinka sink in the netlista netlist if the source is to send both inverting and non-inverting signals from the source to the sink.

2. (Original) The method of claim 1, wherein the moving further comprises:

finding the inverting buffer associated with the source in the netlist;

removing the inverting buffer associated with the source; and

adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes.

3. (Previously presented) The method of claim 2, wherein at least a first route of the plurality of routes is to send the inverting signals from the source to the sink and at least a second route of the plurality of routes is to send the non-inverting signals from the source to the sink.

4. (Original) The method of claim 3, further comprising:

removing the first route.

5. (Original) The method of claim 2, wherein the adding is performed prior to chip placement, timing optimizations, and routing.

6. (Original) The method of claim 2, wherein the adding is performed after chip placement and before timing optimizations and routing.

7. (Currently amended) An apparatus for moving an inverting buffer comprising:

means for interrogating a netlist, wherein the netlist comprises a source, a sink, and an inverting buffer associated with the source; and

means for moving the~~an~~ inverting buffer from the source to the sink in the netlist~~a source to a sink in a netlist~~ if the source is to send both inverting and non-inverting signals from the source to the sink, wherein the means for moving further comprises

means for finding the inverting buffer associated with the source in the netlist,

means for removing the inverting buffer associated with the source, and

means for adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes, and wherein at least a first route of the plurality of routes is to send the inverting signals from the source to the sink and at least a second route of the plurality of routes is to send the non-inverting signals from the source to the sink.

8. (Original) The apparatus of claim 7, further comprising:

means for removing the first route.

9. (Original) The apparatus of claim 7, wherein the means for adding is performed prior to chip placement, timing optimizations, and routing.

10. (Original) The apparatus of claim 7, wherein the means for adding is performed after chip placement and before timing optimizations and routing.

11. (Currently amended) A signal-bearing medium encoded with instructions, wherein the instructions when executed to move an inverting buffer comprise:

interrogating a netlist, wherein the netlist comprises a source, a sink, and the inverting buffer associated with the source; and

moving the~~an~~ inverting buffer from the source to the sink in the netlist~~a source to a sink in a netlist~~ if the source is to send both inverting and non-inverting signals from the source to the sink, wherein the moving further comprises

finding the inverting buffer associated with the source in the netlist,

removing the inverting buffer associated with the source,

adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes, and

removing at least one of the plurality of routes.

12. (Original) The signal-bearing medium of claim 11, wherein the adding is performed prior to chip placement, timing optimizations, and routing.

13. (Original) The signal-bearing medium of claim 11, wherein the adding is performed after chip placement and before timing optimizations and routing.

14. (Original) The signal-bearing medium of claim 11, wherein the source represents a source region in a floorplanned chip and the sink represents a sink region in the floorplanned chip.

15. (Canceled)

16. (Original) The signal-bearing medium of claim 11, wherein the source and sink are in a same subpartition of a chip.

17. (Currently amended) An electronic device for moving an inverting buffer comprising:

a processor; and

a storage device encoded with instructions, wherein the instructions when executed on the processor comprise:

interrogating a netlist, wherein the netlist comprises a source, a sink, and an inverting buffer associated with the source; and

moving thean inverting buffer from the source to the sink in the netlista ~~source to a sink in a netlist~~ if the source is to send both inverting and non-

inverting signals from the source to the sink, wherein the moving further comprises

finding the inverting buffer associated with the source in the netlist,

removing the inverting buffer associated with the source,

adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes, and wherein at least a first route of the plurality of routes is to send inverting signals and at least a second route of the plurality of routes is to send non-inverting signals, and

removing the first route.

18. (Previously presented) The electronic device of claim 17, wherein the source represents a source region in a floorplanned chip and the sink represents a sink region in the floorplanned chip.

19. (Canceled)

20. (Previously presented) The electronic device of claim 17, wherein the source and sink are in a same subpartition of a chip.